

[0060] FIG. 4B illustrates I-V characteristics of the GaN series vertical HEMT of the third embodiment. A drain current slightly flows in an off state.

[0061] According to the third embodiment, since the current blocking layer is made of insulator, leak current passing through the current blocking layer is extremely small. As compared to the current blocking layer made of the p-type GaN layer, the current blocking effect can be apparently improved. As compared to the first and second embodiments, the effect of raising a potential in the lower portion of the non-doped GaN layer 26 by the piezo effect is not provided. Therefore, electrons can move downward from the two dimensional electron gas 2 DEG in an off state, and there is a large possibility that electrons are transported in the GaN layer near the upper surface of the SiO₂ layer 20 and reach the openings.

[0062] Although the invention has been described in conjunction with the embodiments, the invention is not limited to the embodiments. For example, instead of single crystal SiC, single crystal GaN may be used for the substrate. The current blocking layer may be made of insulator other than silicon oxide, such as a silicon nitride and silicon oxynitride. The size, impurity concentration and the like illustratively described above may be changed in various ways. Instead of HEMT, other vertical type field effect transistors may be formed.

[0063] All examples and conditional language recited herein are intended for pedagogical purposes to aid the reader in understanding the invention and the concepts contributed by the inventor to furthering the art, and are to be construed as being without limitation to such specifically recited examples and conditions, nor does the organization of such examples in the specification relate to a showing of the superiority and inferiority of the invention. Although the embodiments of the inventions have been described in detail, it should be understood that the various changes, substitutions, and alterations could be made hereto without departing from the spirit and scope of the invention.

What are claimed are:

1. A compound semiconductor device comprising:
 - a conductive semiconductor substrate;
 - a drain electrode formed on a bottom surface of said conductive semiconductor substrate;
 - a current blocking layer formed on a top surface of said conductive semiconductor substrate, made of high resistance compound semiconductor or insulator, and having openings;
 - an active layer of compound semiconductor burying said openings and extending on an upper surface of said current blocking layer;
 - a gate electrode formed above said openings and above said active layer; and
 - a source electrode laterally spaced from said gate electrode and formed above said active layer.
2. A compound semiconductor device according to claim 1, wherein said conductive semiconductor substrate is made of SiC or GaN, said current blocking layer is made of AlN, and said active layer includes a GaN region.
3. A compound semiconductor device according to claim 2, wherein said active layer includes an n-type AlGaIn layer between said GaN region and said AlN current blocking layer.

4. A compound semiconductor device according to claim 3, wherein said active layer includes an n-type GaN layer formed on said n-type AlGaIn layer, and a non-doped GaN layer formed on said n-type GaN layer.

5. A compound semiconductor device according to claim 1, wherein said conductive semiconductor substrate is made of SiC or GaN, said current blocking layer is made of silicon oxide, and said active layer includes a GaN region.

6. A method for manufacturing a compound semiconductor device comprising:

- (a) forming a current blocking layer on a top surface of a conductive semiconductor substrate, said current blocking layer being made of high resistance compound semiconductor or insulator, and having openings;
- (b) forming an active layer of compound semiconductor burying said openings and extending on an upper surface of said current blocking layer;
- (c) forming a gate electrode above said openings and above said active layer;
- (d) forming a source electrode laterally spaced from said gate electrode and above said active layer; and
- (e) forming a drain electrode on a bottom surface of said conductive semiconductor substrate.

7. The method for manufacturing a compound semiconductor device according to claim 6, wherein:

said conductive semiconductor substrate is made of SiC or GaN;

said step (a) includes:

- (a-1) growing an AlN layer on said conductive semiconductor substrate; and
- (a-2) patterning said AlN layer to form said openings exposing said conductive semiconductor substrate, and

said step (b) includes:

- (b-1) growing a doped GaN layer in an area including said openings; and
- (b-2) growing a non-doped GaN layer on said doped GaN layer.

8. The method for manufacturing a compound semiconductor device according to claim 7, wherein said step (b) includes (b-3) growing a doped AlGaIn layer between said AlN layer and said doped GaN layer.

9. The method for manufacturing a compound semiconductor device according to claim 8, wherein said step (a-1) grows AlN by H-VPE, and said step (b-3) grows AlGaIn by MOCVD.

10. The method for manufacturing a compound semiconductor device according to claim 6, wherein

said conductive semiconductor substrate is made of SiC or GaN;

said step (a) includes:

- (a-1) depositing a silicon oxide layer on said conductive semiconductor substrate; and
- (a-2) patterning said silicon oxide layer to form said openings exposing said conductive semiconductor substrate, and

said step (b) includes:

- (b-1) growing a doped GaN layer in an area including said openings; and
- (b-2) growing a non-doped GaN layer on said doped GaN layer.

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